ABSTRACT OF THE DISCLOSURE

SWITCHING BETWEEN CLOCKS IN DATA PROCESSING

A processor clock control device is disclosed that is operable to control switching between clock signals input to a processor in a glitch-free way. The processor clock control device comprises: at least two clock signal inputs each operable to receive a clock signal, said clock signals comprising a first and a second clock signal; a sensor operable to sense said first and said second clock signals; a clock signal output operable to output a clock signal for input to a processor; and a clock switching signal input for receiving a switching signal operable to control switching of said clock signal output from said first clock signal to said second clock signal; wherein said processor clock control device is operable on receipt of said clock switching signal to sense said first clock signal and when said first clock signal transitions from a first predetermined level to a second level, said processor clock control device is operable to hold said clock signal output at said second level, and then to sense said second clock signal and when said second clock signal transitions from said second level to said first predetermined level to output said second clock signal.

Figure 4